REMARKS/ARGUMENTS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-20 in the application. The Applicants have amended Claims 1, 8 and 15 and have canceled Claims 6, 13 and 20. Accordingly, Claims 1-5, 7-12, and 14-19 are currently pending in the application.

I. Rejection of Claims 1-5, 7-12 and 14 under 35 U.S.C. § 102

The Examiner has rejected Claims 1-5, 7-12 and 14 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,683,547 to DeGroot. The Applicants respectfully traverse the rejection, because DeGroot fails to teach each and every element of Claims 1-5, 7-12 and 14.

DeGroot teaches a floating point unit with an adder pipeline unit and a multiply pipeline unit coupled by a bypass bus. Abstract; Figure 1. "Wait stations" at the input to the adder pipeline unit and the multiply pipeline unit provide a means to hold an operation for which one or more operands are unavailable, while allowing later operations for which all operands are available to complete operation. Figure 1 and column 4, lines 24-31. DeGroot also teaches "unraveling" a loop by an optimizing compiler to make multiple registers available to a number of consecutive instructions in the unraveled loop to increase throughput of the processor. Column 3, line 23, to column 4, line 17.

However, DeGroot does not teach instruction grouping. "Instruction grouping," as the Application uses that term, "determines which instructions can be grouped together for execution in

the same clock cycle." Specification ¶ 39. This definition is consistent with the way in which the term is used in the art.

DeGroot's "unraveled instructions" are not grouped, because they are not constrained to execute in the same clock cycle. Column 3, line 23, to column 4, line 17. Therefore, DeGroot fails to anticipate Claims 1 and 8.

For the sake of argument, even were DeGroot to teach grouping in a general way, DeGroot still does not anticipate the element of "a processor having ... instruction grouping logic" as Claims 1 and 8 recite. In ¶ 8 of the Action, the Examiner asserts that various portions of DeGroot anticipate these elements, without citing any portions specifically. However, a detailed study of DeGroot finds that it is silent with respect to instruction grouping logic on a processor. If the Examiner disagrees, the Applicants respectfully request that she provide an unambiguous reference to those specific portions of DeGroot that support her assertion. In the absence of that support, DeGroot does not teach a processor having instruction grouping logic and fails to anticipate Claims 1 and 8.

For at least the reasons set forth above, DeGroot does not anticipate the invention, and Claims 1 and 8 are allowable. Furthermore, as the dependent claims include the limitations of the base claims, Claims 2-5, 7, 9-12, and 14 are also allowable. Accordingly, the Applicants respectfully request the Examiner to withdraw the rejection under 35 U.S.C. § 102(b) with respect to these claims.

II. Rejection of Claims 15-19 under 35 U.S.C. § 103

The Examiner has rejected Claims 15-19 under 35 U.S.C. § 103(a) as being unpatentable over DeGroot in view of U.S. Patent No. 4,683,547 to Chamdani, *et al.* The Applicants respectfully traverse the rejection, because the combination of DeGroot and Chamdani, taken in combination, fails to teach each and every element of independent Claim 15. Specifically, the combination fails to teach grouping of instructions for execution in a single clock cycle.

As set forth above, DeGroot teaches generally a floating point unit with an adder pipeline unit and a multiply pipeline unit coupled by a bypass bus. As further set forth, DeGroot also teaches "unraveling" an instruction loop by an optimizing compiler. Chamdani is concerned with a scheme for a distributed instruction queue (DIQ). Abstract. A DIQ allows a reduction of the number of global wires in the processor. Id. The Examiner cites Chamdani at column 2, lines 10-12 for his teaching of multi-instruction issue. Examiner's Response, ¶ 14. However, Chamdani does not teach grouping of instructions for execution in the same clock cycle, as Claim 15 recites. Chamdani places several constraints on instruction groups, but makes no mention whatsoever as to the timing of the execution of the instructions, much less that they be executed in the same clock cycle. Column 31, lines 2-24. Therefore, the combination of DeGroot and Chamdani does not teach "said grouping logic groups said multiply-accumulate instructions for execution in a single clock cycle" and fails to support a *prima facie* case of obviousness of Claim 15.

Independent Claim 15 is therefore allowable under 35 U.S.C. § 103(a). Furthermore, because Claims 16-19 include the limitations of Claim 15, these claims are also allowable. The Applicants therefore respectfully request the Examiner withdraw the rejection of Claims 15-19.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-5, 7-12 and 14-19.

The undersigned does not believe that any fees are due regarding this matter. However, the undersigned hereby authorizes the Commissioner to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 08-2395.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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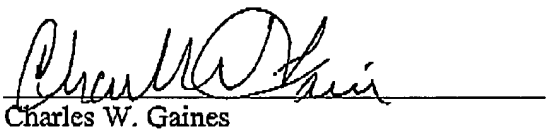

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Dated: November 18, 2005

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